

**Patent Number:** 

[11]

#### US005977587A

# United States Patent [19]

[45] **Date of Patent:** Nov. 2, 1999

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Kito

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A perimeter gate wiring 52 comprises a contact portion 54

[54]	SEMICONDUCTOR DEVICE AND A
	METHOD FOR WIRING OF A
	SEMICONDUCTOR DEVICE

Primary Examiner—Olik Chaudhuri Assistant Examiner—Phat X. Cao

[75] Inventor: Takayuki Kito, Kyoto, Japan[73] Assignee: Rohm Co., Ltd., Kyoto, Japan

Assistant Examiner—Phat X. Cao Attorney, Agent, or Firm—Darby & Darby

[21] Appl. No.: **08/672,978** 

[57] ABSTRACT

[22] Filed: Jul. 1, 1996

[56]

and an interconnecting portion 56 having narrower width than the contact portion 54 which connects the contact portion 54 mutually. And the perimeter gate wiring 52 is connected electrically with the gate perimeter portion 66 at the contact portion 54. A source wiring perimeter portion 58 comprises a contact portion 60 and an interconnecting portion 62 having narrower width than the contact portion 60 which connects the contact portion 60 mutually. And the source wiring perimeter portion 58 is connected electrically with a perimeter diffusion layer 74 in the contact portion 60. The contact portion 54 of the perimeter gate wiring 52 and the interconnecting portion 62 of the source wiring perimeter portion 58 are provided adjacently. Also, the interconnecting portion 56 of the perimeter gate wiring 52 and the contact portion 60 of the source wiring perimeter portion 58 are provided with one another adjacently. So that, it is possible to narrow a width of both the perimeter gate wiring 52 and the source wiring perimeter portion 58 with main-

[30]	Fore	eign A	pplicat	ion Priority Data	
Jun.	29, 1995	[JP]	Japan		7-163321
[51]	Int. Cl. <sup>6</sup>			<b>H01L 29/76</b> ; H01 H01L 31/062; H01	

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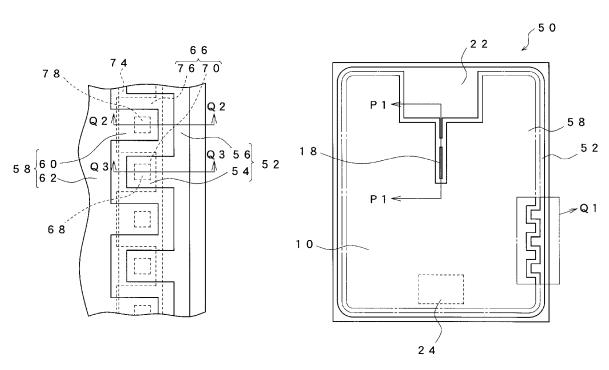
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## 12 Claims, 14 Drawing Sheets

taining contact between the gate perimeter portion 66 and



the like.